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Design and Comparison of 1 Bit Full Adder in GPDK 180nm & 45 Nm Technology

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ABSTRACT: Adders are the basic building blocks in digital computer systems. Arithmetic operations are widely used in most digital computer systems. Addition is a fundamental arithmetic operation and is the base for arithmetic operations such as multiplication and the basic adder cell can be modified to function as subtractor by adding another xor gate and can be used for division. Therefore, 1-bit Full Adder cell is the most important and basic block of an arithmetic unit of a system. Hence in order to improve the performance of the digital computer system one must improve the basic 1-bit full adder cell.There is always a trade-off between speed and power dissipation in VLSI Design.

In this project, various types of full adder designs are performed.3T XOR with MUX logic is used in 8 transistor full adder.4T XNOR with MUX logic is used in 10 transistor full adder.12 transistor full adder is designed using multiplexers & 14 transistor is designed using 6T XNOR. Different techniques are used for low power in full adders. Analysis is based on some simulation parameters like number of transistors, power, delay and different technologies (45nm & 180nm technologies) at different supply voltages.

1. INTRODUCTION

Additions are basic arithmetic operations. It is mainly used in lot of VLSI system such as microprocessors and application specific DSP architecture. In addition its main task is adding two numbers, it is used in many other useful operations such as, subtraction, multiplication, address calculation, etc. Building low power VLSI system has emerged as significant performance goal because of the fast technology in mobile communication and computation. The developments in battery technology have not taken place as fast as the advances in electronic devices. So the developers are attained with more; high speed, high throughput and at the same time, low power consumption as possible.

In electronics,adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Although adders can be constructed for many numerical representations, such as binary-coded decimal, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subtractor. Other signed number representations require a more complex adder Full adder is one of the most critical components of a processor, as it is used in the Arithmetic Logic Unit (ALU), in the floating-point unit and for address generation in case of cache or memory access. Several refinements has been made regarding its structure since its invention. The main aim of those modifications is to reduce the number of transistors to be used to perform the required logic, reduce the power consumption and increase the speed of operation. One of the major advantages in reducing the number of transistors is to put more devices on a single silicon chip there by reducing the total area.

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In the recent days the use of portable electronic devices like cellular devices, laptops has been increased exponentially. The main requirement of these portable devices is reduced power consumption, small area and high speed of operation. To achieve these requirements research efforts in the field of low power VLSI (very large scale integration) have increased many folds. As the number of transistors on a single silicon chip increases, the package density also increases. With the rise in chip density, power consumption of VLSI systems is also increasing and this further, adds to reliability and packaging problems. Packaging and cooling cost of VLSI systems also goes up with high power dissipation. So, the low power consumption along with minimum delay and area requirements is one of important design consideration for IC designers in designing portable electronic devices and many sophisticated hardware circuits.

II. SSI, LSI, MSI AND VLSI

Small scale (SSI), medium scale (MSI), and large scale (LSI) integrated circuits (ICs) have been a main stay of digital logic circuit implementation for more than forty years. They are still in use for educational purposes and for small to medium sized industrial projects that will be constructed in small quantities or for special purpose applications. ICs are interconnected using wires or printed circuit boards in order to realize the desired functionality. Circuits constructed of SSI, MSI, and LSI ICs are generally referred to as fixed logic since the functions they realize cannot be changed without physically rebuilding the circuit. So design changes are difficult, expensive, or impossible. The advent of very large scale integrated (VLSI) circuits led to the development of programmable and customizable logic devices which were introduced about twenty-five years ago and have grown in popularity because of their cost effectiveness, versatility, ease of design change, and the availability of computer-aided-design (CAD) software to support the design process. Programmable devices also enable the design and implementation of much larger and more complex systems. Currently, field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), and microcontrollers are the most commonly used of these type devices.

➢SSI – Small Scale Integration

It has less than 100 components (about 10 gates).The first integrated circuits contained only a few transistors and so were called “small-scale integration (SSI). They used circuits containing transistors numbering in the tens. They were very crucial in development of early computers. SSI was followed by introduction of the devices which contained hundreds of transistors on each chip, and so were called “medium scale integration (MSI).

➢MSI – Medium Scale Integration·

It contains less than 500 components or has more than 10 but less than 100 gates. They were attractive economically because which they cost little more systems to be produced using smaller circuit boards, less assembly work, and a number of other advantages. Next development was of LSI.

➢LSI – Large Scale Integration·

Here number of components is between 500 and 300000 or have more than 100 gates. The development of LSI was driven by economic factors and each chip comprised tens of thousands of transistors. It was in 1970s, when LSI started getting manufactured in huge quantities. LSI was followed by VLSI where “very large-scale integration”(VLSI)

➢VLSI – Very Large Scale Integration

The concept of Very-Large-Scale Integration (VLSI) was coined more than thirty years ago to describe the process of conceiving, designing and fabricating integrated circuits by combining thousands of transistors and their interconnections in a single chip. This happened when the available MOS technologies had a feature size larger than 1 μm.

As technology evolved towards smaller sizes, decreasing more and more, the term VLSI was applied to chips formed by hundreds of thousands and even hundreds of millions of transistors.

Historically, the first integrated circuits consisted only of a few components, making it possible to fabricate one or more logic gates on a single device, in what is now retrospectively known as Small-Scale Integration (SSI). Afterwards, further improvements in technology led to chips with hundreds of logic gates, the so-called Medium-Scale Integration (MSI), and even more than thousand logic gates (large-scale integration or LSI).

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The main reasons why we are preferring VLSI are

A) Greater Functionality Its results in average energy savings of 35% to 70%with an average speed up of 3 to 7 times.

B) After fabrication many applications could share commodity economics for the production of a single IC and the same IC could be used to solve different problems at different points in time.

C) Lower System Cost by eliminating the ASIC design lower system cost on a low volume product is archived

III. PROPOSED WORK

A basic cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (A, B, and Cin) and two 1-bit outputs (sum and carry). The relations between the inputs and the outputs are expressed as: SUM= ⊕⊕ CARRY=AB+(⊕)C The table giving the outputs for each input combination. Each row of the table is filled in simply by writing in binary the sum of the three bits A + B + C, using 0 = 00, 1 = 01, 2 = 10, and 3 = 11. Upon inspection of this table, we can see that the sum bit S = 1 whenever an odd number of input bits are equal to 1. A Boolean function that can provide this result is the exclusive-OR, XOR, symbolized by A ⊕ B, which is 1 if either A or B is 1, but not both. It is easy to verify that SUM. (The parentheses could be omitted, since XOR is an associative operator.) The carry-out is 1 whenever a majority of inputs are 1. A clever way to implement this is as carry

.

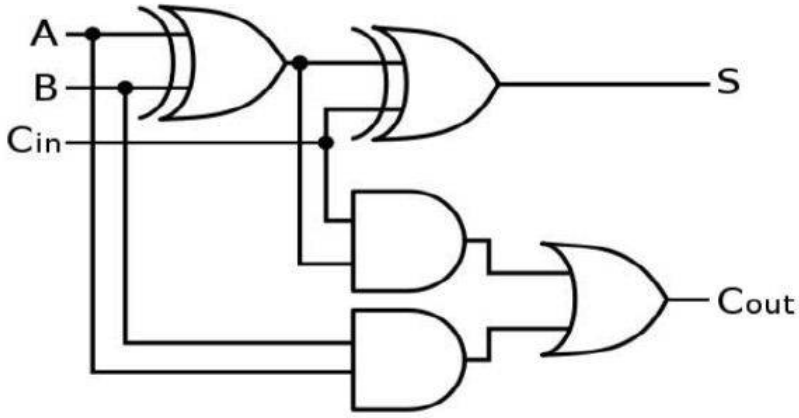

Fig.3.1.: Logic diagram of full adder

TRUTH TABLE (Full Adder - 1bit)

X	Y	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 3.1.: Truth table of full adder

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IV.RESULTS

4.1. Transient response:

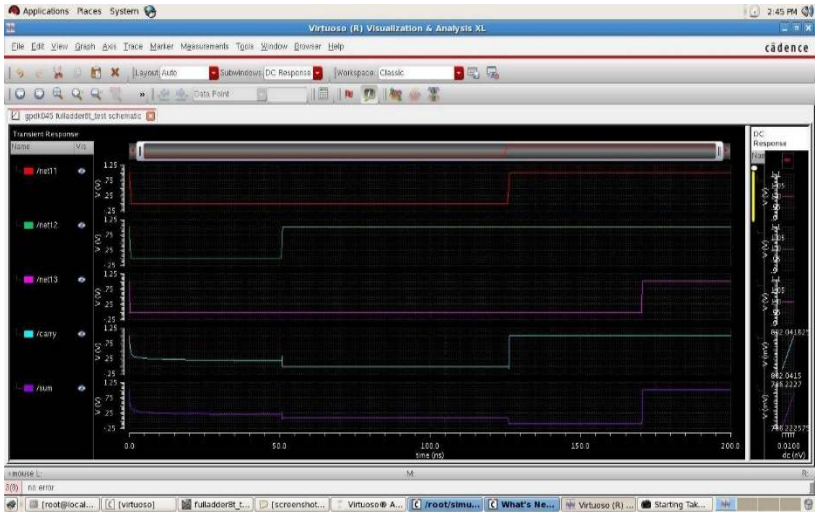

Fig.4.1.: Transient response of 8T full adder

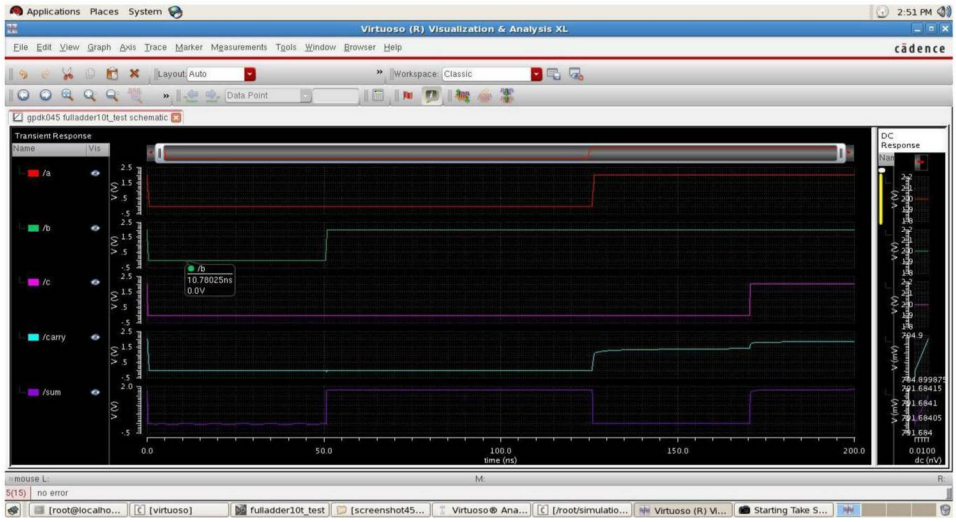

Fig.4.2.: Transient response of 10T full adder

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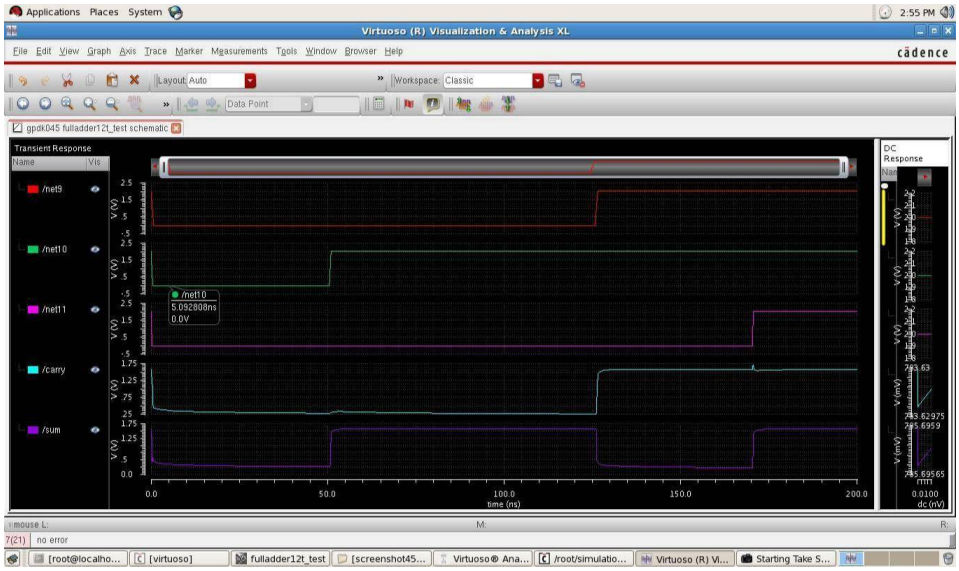

Fig.4.3.: Transient response of 12T full adder

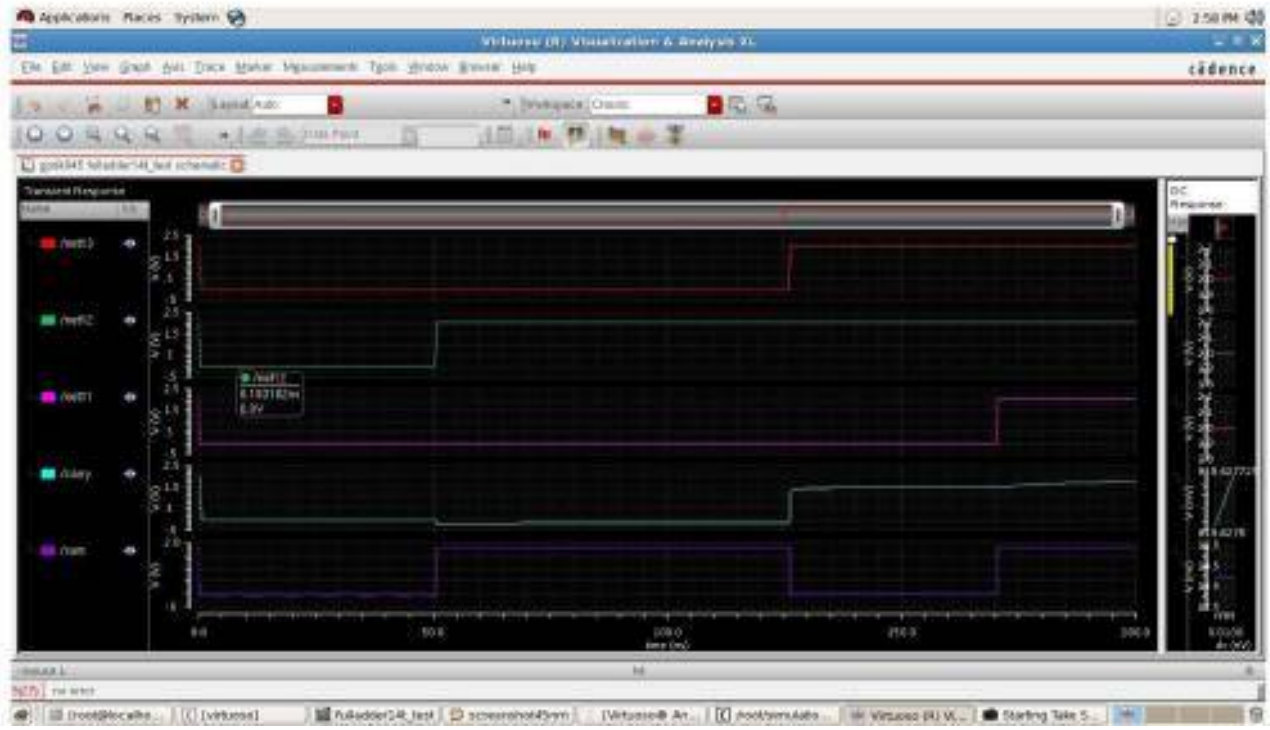

Fig.4.4.: Transient response of 14t full adder

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- Delay is measured as:

$$df = t(vo<Vdd/2)-t(vi>Vdd/2)$$

$$dr = t(vo>Vdd/2)-t(vi<Vdd/2)$$

$$d = davg=(dr + df)/ 2$$

Where,df and dr are falling and raising output propogation delays.

- Total power= dynamicpower +stactic power +short circuit power

Dynamic power=αfC(Vdd)^2
Static power=Vdd*Idd
Short circuit power=αfVdd*F(input transition,output transition)
Where, α=activity factor
F=input frequency
C=total capacitance

- Delay is measured as:

df = t(vo<Vdd/2)−t(vi >Vdd/2)
dr = t(vo>Vdd/2)−t(vi <Vdd/2)
d = davg=(dr + df)/ 2
Where,df and dr are falling and raising output propagation delays.

- Total power= dynamic power +static power +short circuit power

Dynamic power=αfC(Vdd)^2
Static power=Vdd*Idd
Short circuit power=αfVdd*F(input transition,output transition)
Where, α=activity factor
F=input frequency
C=total capacitance

ESTIMATION OF DELAY & POWER CONSUMPTION

- For 10T, df = t(vo<Vdd/2)−t(vi >Vdd/2)=95ns-150ns=55ns dr = t(vo>Vdd/2)−t(vi <Vdd/2)=105ns - 50ns=55ns d = davg =(dr + df)/ 2 =55ns

- Power=23.26µW
Static=Vdd*Idd=8.9pW
Dynamic= αfC*(Vdd)^2=0.2µW
Short circuit= αfVdd*F(input transition,output transition) =0.4pW

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4.2. DESIGN AND COMPARISION OF 1 BIT FULL ADDER IN GPDK 180NM & 45 NM TECHNOLOGY IN 180nm & 45nm *(Channel length of transistor)* TECHNOLOGY

Table 4.1.: Comparison of different full adder results

		8T FULL ADDER	10T FULL ADDER	12T FULL ADDER	14T FULL ADDER
NO. OF TRANSISTORS		8	10	12	14
DELAY	180nm	170.8ns	51.58ns	50.5ns	127ps
	45nm	170.5ns	50.81ns	50.87ns	50.61 ns
TOTAL POWER CONSUMPTION		5.39nW	23.26µw	62.02nW	83.87 µW
	45nm	25.25pW	6.27nW	401.5pW	15.97 µW

V.CONCLUSION & FUTURE SCOPE

In this project, we have designed various full adders and verified the simulation results of every full adder. Delay and power consumption of different full adders (8 transistor (8T),10 transistor (10T),12 transistor (12T) & 14 transistor (14T)) in both 180nm & 45nm technology are compared.

As Full adder is the basic building block of the ALU,by optimizing the performance of ALU,one can optimize the performance of processors. Reducing the transistor count,the delay and power consumption of the full adder to an extent.Channel length (in nm) has a great impact on the power consumed by the circuit.By varying the channel length of the transistor,the characteristics of the full adder can be varied.

The threshold loss problem in the full adder can be reduced by further varying the parameters of the full adder i.e.,supply,channel length,number of transistors.

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